WHAT IS CLAIMED IS:

1. A method of forming semiconductor devices having field oxides in trenches, comprising:

providing a semiconductor substrate;

forming an upper trench at a predetermined region of the semiconductor substrate and a bottom trench at a bottom surface of the upper trench; the upper trench having a wider width than the bottom trench, and

forming a field oxide filling the bottom trench and the upper trench.

2. The method as claimed in claim 1, wherein forming the upper trench and bottom trench comprises:

forming an assistant trench at a predetermined region of the semiconductor substrate;

forming a trench mask layer on the semiconductor substrate having the assistant trench;

forming an opening exposing the assistant trench and a predetermined region of the semiconductor substrate at both sides of the assistant trench by patterning the trench mask layer; and

forming the upper trench and the bottom trench by anisotropically etching the exposed bottom surface of the assistant trench and the semiconductor substrate,

wherein the upper trench has substantially the same width as the opening and the bottom trench has substantially the same width as the assistant trench.

3. The method as claimed in claim 2, further comprising forming a channel stop impurity-doped region in the semiconductor substrate apart from the bottom surface of the assistant trench with a predetermined depth, wherein the bottom surface of the bottom trench is in contact with the channel stop impurity-doped region.

4. The method as claimed in claim 3, wherein the assistant trench has substantially the same width as the channel stop impurity-doped region.

5. The method as claimed in claim 4, wherein forming the assistant trench and the channel stop impurity-doped region comprises:

forming an assistant trench mask layer on the semiconductor substrate;

forming an assistant trench opening exposing a predetermined region of the semiconductor substrate by patterning the assistant trench mask;

forming an assistant trench by selectively etching the exposed semiconductor substrate;

forming a channel stop impurity-doped region in the semiconductor substrate apart from the bottom surface of the assistant trench with a predetermined depth by implanting impurity ions using the patterned assistant trench mask layer as a mask; and

removing the patterned assistant trench mask layer.

6. The method as claimed in claim 3, wherein the assistant trench has a wider width than the channel stop impurity-doped region.

7. The method as claimed in claim 6, wherein forming the channel stop impurity-doped region comprises:

forming an ion-implantation mask layer on the semiconductor substrate having the assistant trench;

forming an ion-implantation opening having a narrower width than the assistant trench and exposing a bottom predetermined region of the assistant trench by patterning the ion-implantation mask layer;

forming a channel stop impurity-doped region in the semiconductor substrate apart from the bottom surface of the assistant trench by implanting impurity ions using the patterned ion-implantation mask as a mask; and

removing the patterned ion-implantation mask.

8. The method as claimed in claim 2, wherein forming the field oxide comprises:

forming a field insulator filling the upper trench and the bottom trench on a surface of the semiconductor substrate;

planarizing the field insulator until the patterned trench mask layer is exposed; and

removing the exposed trench mask layer.

9. The method as claimed in claim 1, wherein forming the upper trench and the bottom trench comprises:

forming an upper trench at a predetermined region of the semiconductor substrate; and

forming a bottom trench by selectively etching a bottom predetermined region of the upper trench.

10. The method as claimed in claim 9, further comprising forming a channel stop impurity-doped region in the semiconductor substrate under the bottom trench, wherein the bottom surface of the bottom trench is in contact with the channel stop impurity-doped region.

11. The method as claimed in claim 9, wherein the assistant trench has an identical or wider width than the channel stop impurity-doped region.

12. A method of forming semiconductor devices having field oxides in trenches comprising:

providing a semiconductor substrate having a first region and a second region;

forming a first trench at a predetermined region of the semiconductor substrate at the first region and a second trench composed of an upper trench at a predetermined region of the semiconductor substrate at the second region and a bottom trench at the bottom of the upper trench; and

forming a first field oxide filling the first trench and a second field oxide filling the second trench,

wherein the first trench and the upper trench have identical depths from a surface of the semiconductor substrate and the upper trench has a wider width than the bottom trench.

13. The method as claimed in claim 12, wherein forming the first trench and the second trench comprises:

forming an assistant trench at a predetermined region of the semiconductor substrate at the second region;

forming a trench mask layer on the semiconductor substrate having the assistant trench;

patterning the trench mask layer to form a first opening exposing a predetermined region of the semiconductor substrate at the first region and a second opening exposing the assistant trench and a predetermined region of the semiconductor substrate at both sides of the assistant trench at the second region; and

anisotropically etching the semiconductor substrate and a bottom surface of the assistant trench exposed by the first opening and the second opening to form the first trench and the second trench ,

wherein the upper trench has substantially the same width as the second opening and the bottom trench has substantially the same width as the assistant trench.

14. The method as claimed in claim 14, wherein after forming the assistant trench, the method further comprising forming a channel stop impurity-doped region in the semiconductor substrate apart from a bottom surface of the assistant trench with a predetermined depth, wherein a bottom surface of the bottom trench is in contact with the channel stop impurity-doped region.

15. The method as claimed in claim 14, wherein the assistant trench has substantially the same width as the channel stop impurity-doped region.

16. The method as claimed in claim 15, wherein forming of the assistant trench and the channel stop impurity-doped region comprises:

forming an assistant trench mask layer on the semiconductor substrate;

forming an assistant trench opening exposing a predetermined region of the semiconductor substrate at the second region by patterning the assistant trench mask layer;

forming an assistant trench by etching the exposed semiconductor substrate;

forming a channel stop impurity-doped region in the semiconductor substrate apart from a bottom surface of the assistant trench with a predetermined region by implanting impurity ions using the patterned assistant mask layer as a mask; and

removing the patterned assistant trench mask layer.

17. The method as claimed in claim 14, wherein the assistant trench has a wider width than the channel stop impurity-doped region.

18. The method as claimed in claim 17, wherein forming the channel stop impurity-doped region comprises:

forming an ion-implantation mask layer on the semiconductor substrate having the assistant trench;

forming an ion-implantation opening having a narrower width than the assistant trench and exposing a predetermined region of a bottom surface of the assistant trench by patterning the ion-implantation mask layer;

forming a channel stop impurity-doped region in the semiconductor substrate apart from a bottom surface of the assistant trench with a predetermined depth by implanting impurity ions using the patterned ion-implantation mask layer as a mask; and

removing the patterned ion-implantation mask layer.

19. The method as claimed in claim 12, wherein forming the first trench and the second trench comprises:

forming a first trench at a predetermined region of the semiconductor substrate at the first region and an upper trench at a predetermined region of the semiconductor substrate at the second region; and

forming a bottom trench by selectively etching a predetermined region of a bottom surface of the upper trench.

20. The method as claimed in claim 19, further comprising forming a channel stop impurity-doped region under a bottom surface of the bottom trench, wherein the bottom surface of the bottom trench is in contact with the channel stop impurity-doped region.

21. The method as claimed in claim 20, wherein a width of the bottom trench is equal to or wider than that of the channel stop impurity-doped region.

22. A method of forming semiconductor devices having field oxides in trenches comprising:

providing a semiconductor substrate having a first region, a second region and a key region;

forming an assistant trench at a predetermined region of a semiconductor substrate at the second region and an initial key trench at a predetermined region of the semiconductor substrate at the key region;

forming a trench mask layer on a surface of the semiconductor substrate having the assistant trench and the key trench;

patterning the trench mask layer to form a first opening exposing a predetermined region of the semiconductor substrate at the first region, a second opening exposing the

assistant trench and a predetermined region of the semiconductor substrate at both sides of the assistant trench the second region and a key opening exposing the initial key trench and a predetermined region of the semiconductor substrate at the key region;

anisotropically etching the bottom surface of the assistant trench and the exposed semiconductor substrate to form a first trench at the first region, a second trench composed of an upper trench at a surface of the semiconductor substrate at the second region and a bottom trench at a bottom surface of the upper trench, and a key trench composed of an upper key trench at a surface of the semiconductor substrate at the key region and a bottom key trench at a bottom surface of the upper key trench; and

forming a first field oxide in the first trench, a second field oxide in the second trench and a key field oxide in the key trench.

Wherein the first trench, the upper trench and the upper key trench have identical depths from a surface of the semiconductor substrate, the upper trench has substantially the same width as the second opening and the bottom trench has substantially the same width as the assistant trench.